ispLSI® 8840 OE and Internal Tristate Configuration

Introduction

This document provides a detailed description of the ispLSI 8840 internal tristate bus and the output enable control configuration. It is assumed that the reader is familiar with the ispLSI 8840 architecture. Refer to the ispLSI 8840 data sheet for additional architectural information.

The internal tristate bus spans across the Global Routing Plane and is driven from the GLB outputs or the global I/O cells.

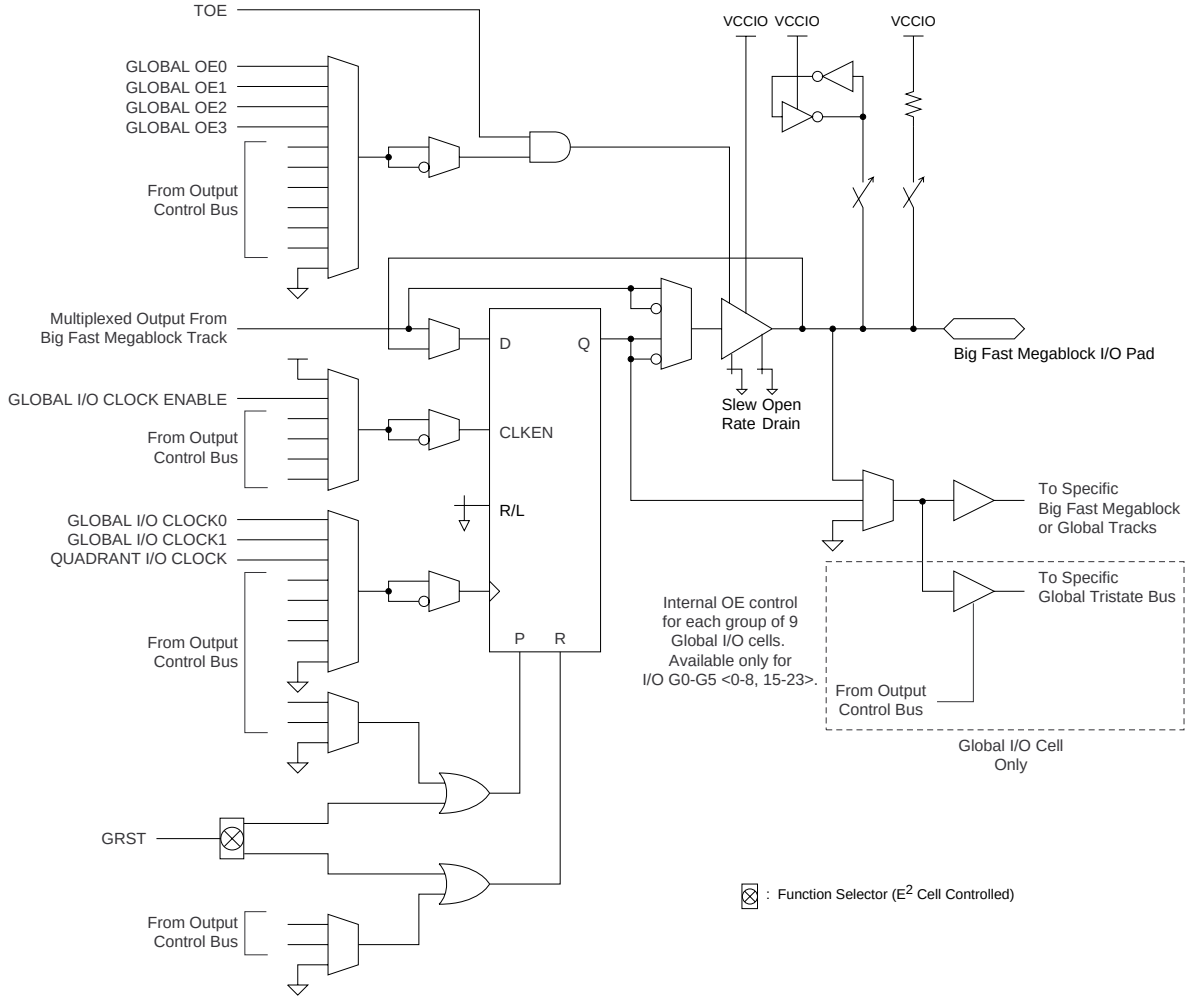
The output enable control of the I/O cells can originate from one of three sources: TOE, Global OE input pin or internal logic that drives the Output Control Bus.

Internal Tristate Bus

The internal tristate buses are grouped in the same manner as the Global I/O grouping described in the pin location table of the ispLSI 8840 data sheet. Eighteen Global I/O cells, I/O G0-G5 <0-8, 15-23>, as described in the I/O pin location table of the data sheet, are capable of driving the 18-bit wide internal tristate bus as well as the Global Routing Plane. The Global I/O cells, I/O G0-G5 <9-14>, only drive the Global Routing Plane. Figure 1 illustrates the Global I/O cell. The internal OE control for each group of nine Global I/O cells is driven from the same output control bus signal.

The internal tristate bus can also be driven from any of the GLB outputs that span across all Big Fast Megablocks

Figure 1. ispLSI 8840 Global I/O Cell



(BFMs). Each corresponding GLBs across all BFMs can drive the common 18-bit internal tristate bus as well as the routing planes. The same 18-bit internal tristate bus can also be driven from the corresponding Global I/O cells (see Figure 2).

The ispLSI 8840 has a total of 108 internal tristate buses that are accessible either from the GLBs or the Global I/O cells. Each Global I/O internal OE control signal can control up to a 9-bit wide internal tristate bus. The internal OE for the Global I/O comes from the output control bus. In the case of the GLB, internal OE control is generated from the OE control macrocells of the GLB as shown in Figure 3. The GLB internal OE can control up to 9-bit or 18-bit wide internal tristate buses. Any smaller granularity bus width control is also possible by selecting the internal OE control at the individual OE control multiplexor described in Figure 3. The individual OE multiplexor selects between the internal OE control from one of two macrocells or always output enabled. The embedded tristate bus has internal bus hold and arbitration features in order to make the function more "user friendly." The bus hold feature keeps the internal bus at the previously driven logic state when the bus is not driven to eliminate bus float. The bus arbitration is performed on a "first come first served" priority. In other words, once a logic block drives the bus, other logic blocks cannot drive the bus until the first releases the bus. This arbitration feature prevents internal bus contention when there is an overlap between two bus enable signals. Typically, it takes about 3ns to resolve one bus signal coming off the bus to another bus signal driving the bus. The arbitration feature combined with the predictability of CPLD, makes

Figure 2. ispLSI 8840 Internal Tristate Bus

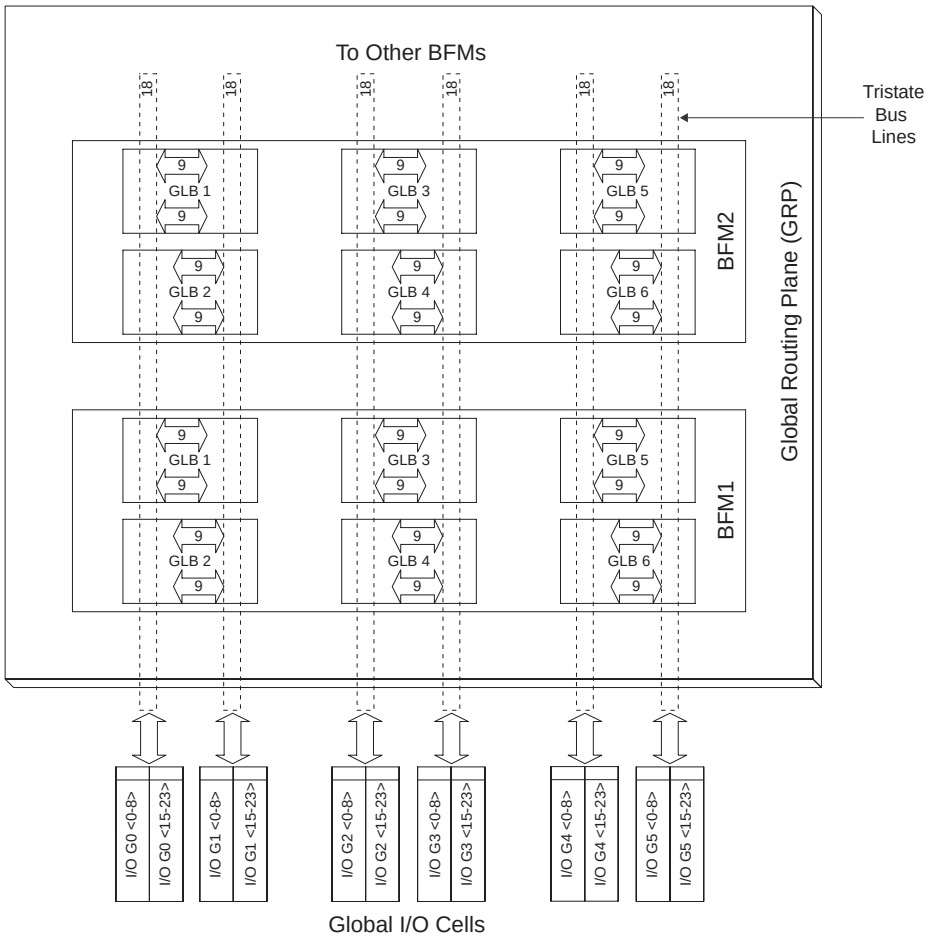
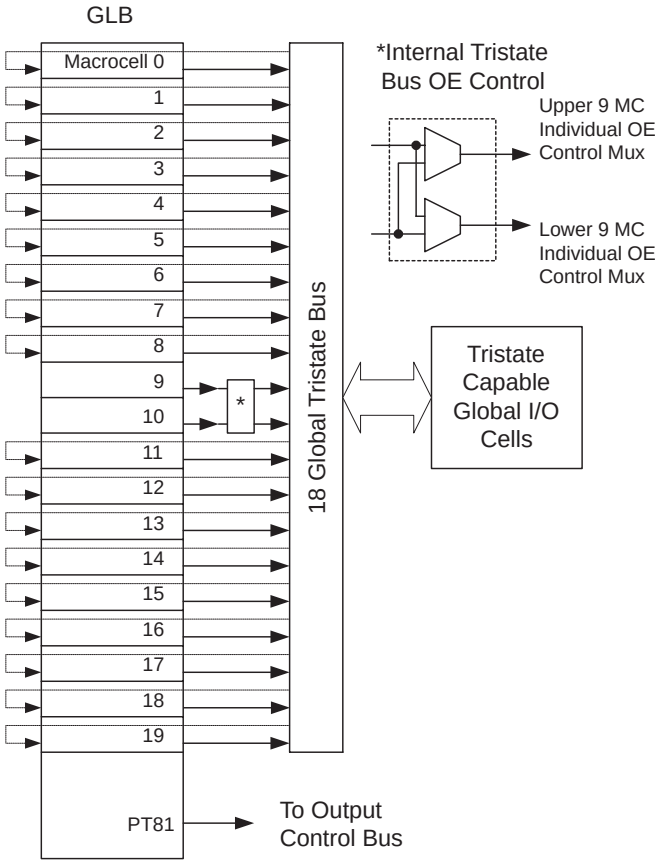


Figure 3. ispLSI 8840 GLB Tristate Bus and OE Control Block Diagram



the embedded tristate bus the most practical for the real world bus implementations.

The internal tristate bus can be thought of as an extension of the I/O pins with OE control. Any external signal buses can be brought inside of the device. Since the tristate bus signals can be fed directly into the macrocell registers, the link between common functions that span across a BFM can bypass the routing planes. By bringing the external buses inside the device, the I/O utilization will dramatically decrease. An example of this is two sets of eight-bit macrocell outputs that are connected to eight Global I/O Pins on the internal tristate bus. Without the internal tristate bus, this implementation would require 16 I/O pins with OE control.

Output Control Organization

In addition to the data input and output to the I/O cells, each I/O cell can have up to six different I/O cell control signals. In addition to the internal OE control, the five control signals for each I/O cell consist of pin OE control, clock enable, clock input, asynchronous preset and asynchronous reset. All of the I/O control signals can be driven either from the dedicated external input pins or from the internal control bus.

The output enable of each I/O cell can be driven by 21 different sources: 16 from the output control bus, four from the Global OE pins and one from the Test OE pin. The Global OE signals and Test OE signal are driven from the dedicated external control input pins.

The 16-bit wide output control buses are organized in four different quadrants as shown in Figure 4. Since each GLB is capable of generating the output control signals, each of the output control bus signals can be driven from a unique GLB. The 42 GLBs can generate a total of 42 unique I/O control signals. Referring to Figure 3, the GLB generates its output control signal the control product term (PT81).

Figure 4 also illustrates how the quadrant clocks are routed to the appropriate quadrant I/O cells.

Figure 4. Output Control Bus and Quadrant Organization